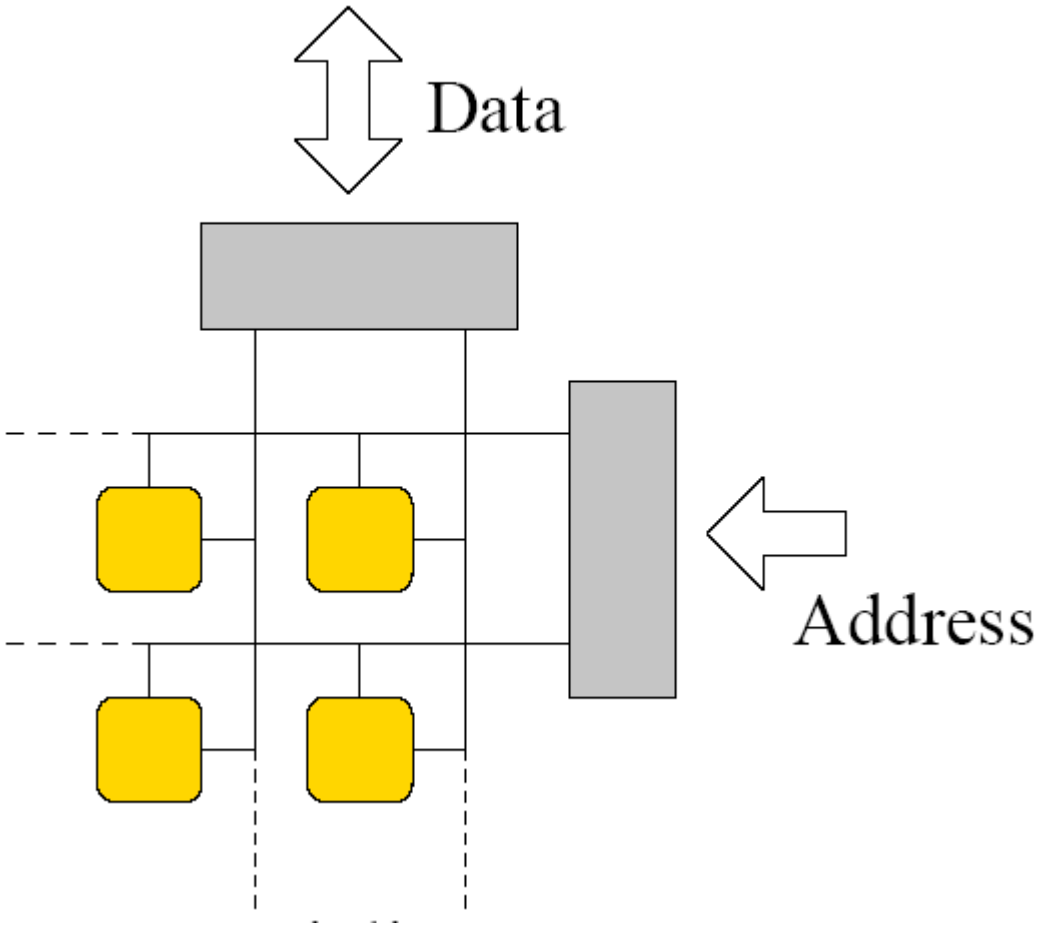
Semiconductor Memory

LECTURE 23

- memory organization
- memory-density trends
- flash memory
- DRAM

Chap. 15

Memory organization



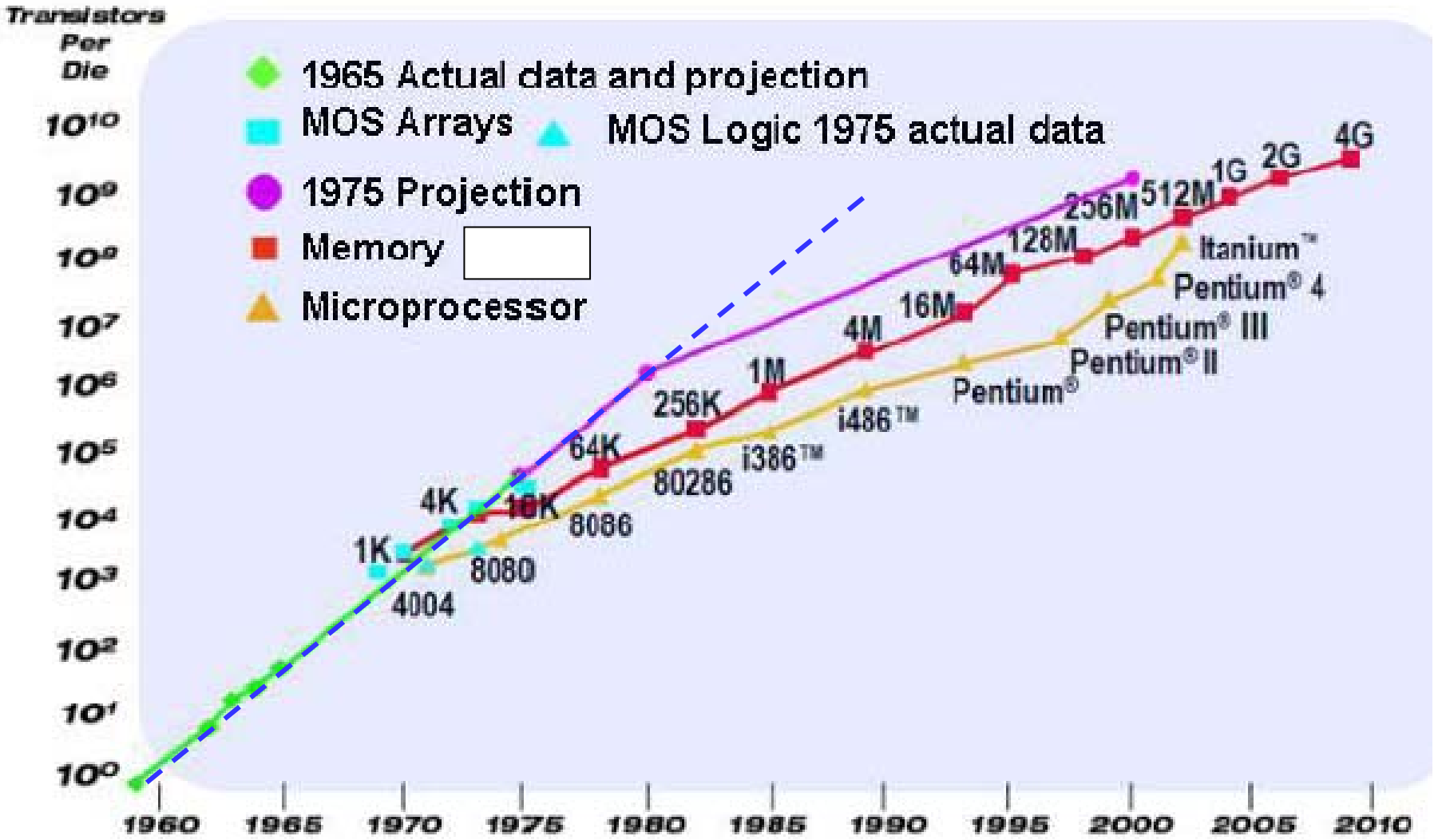
Identify:

- Memory cells
- Word lines
- Bit lines
- Decoder
- MUX/DEMUX

Industry strives to make cells as [ ] as possible.

Sketch a MOST memory cell, showing word- and bit-line connections

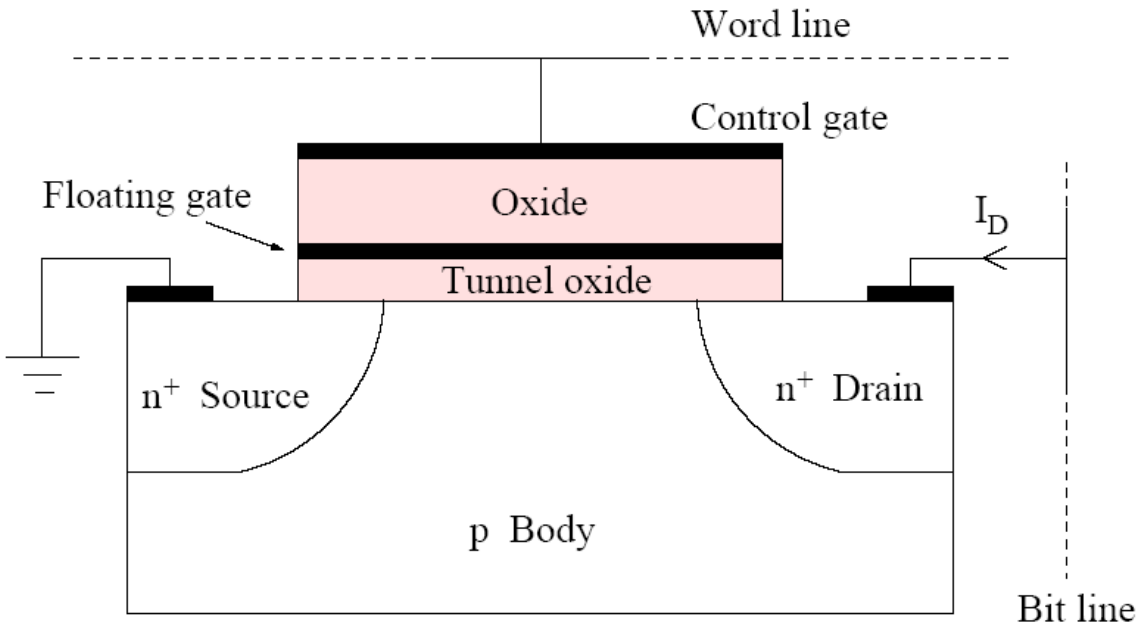
Memory Density



Hans Moravec, CMU

Sec. 15.1

Flash memory cell



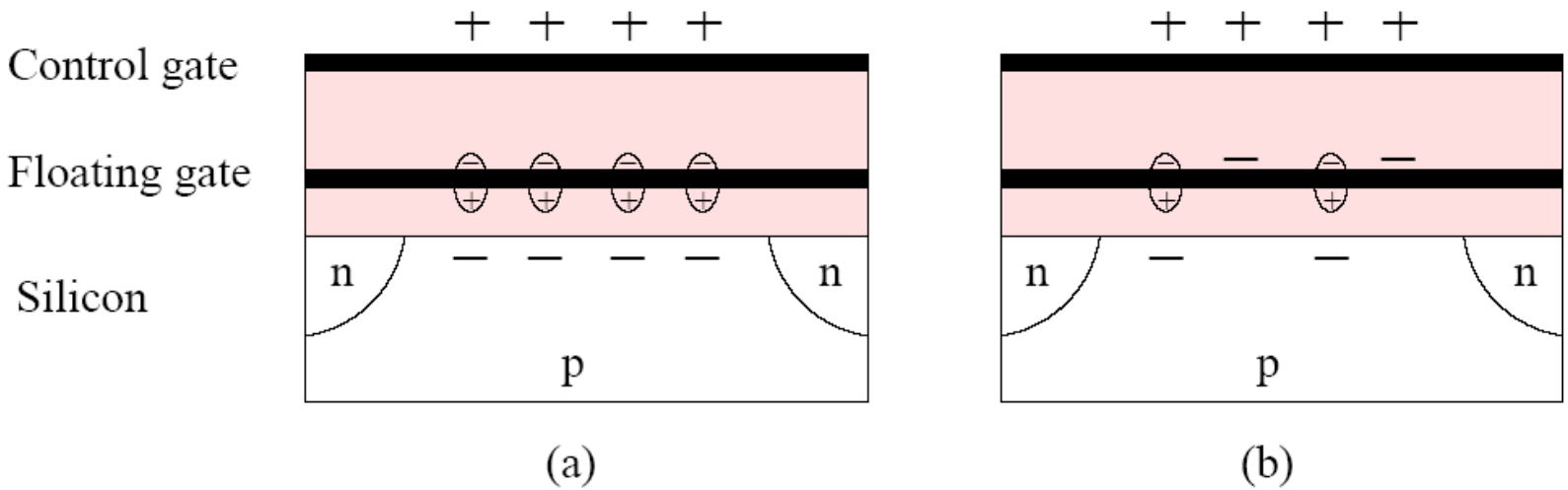
What is the most significant difference from a regular MOSFET?

How is the cell programmed (written and erased)?

How is the cell read?

Sec. 15.1

Charge on Floating Gate



Let Q_n=-4q represent inversion.

Enable word line.

Does the bit-line sense an I_D in (a) and/or (b)?

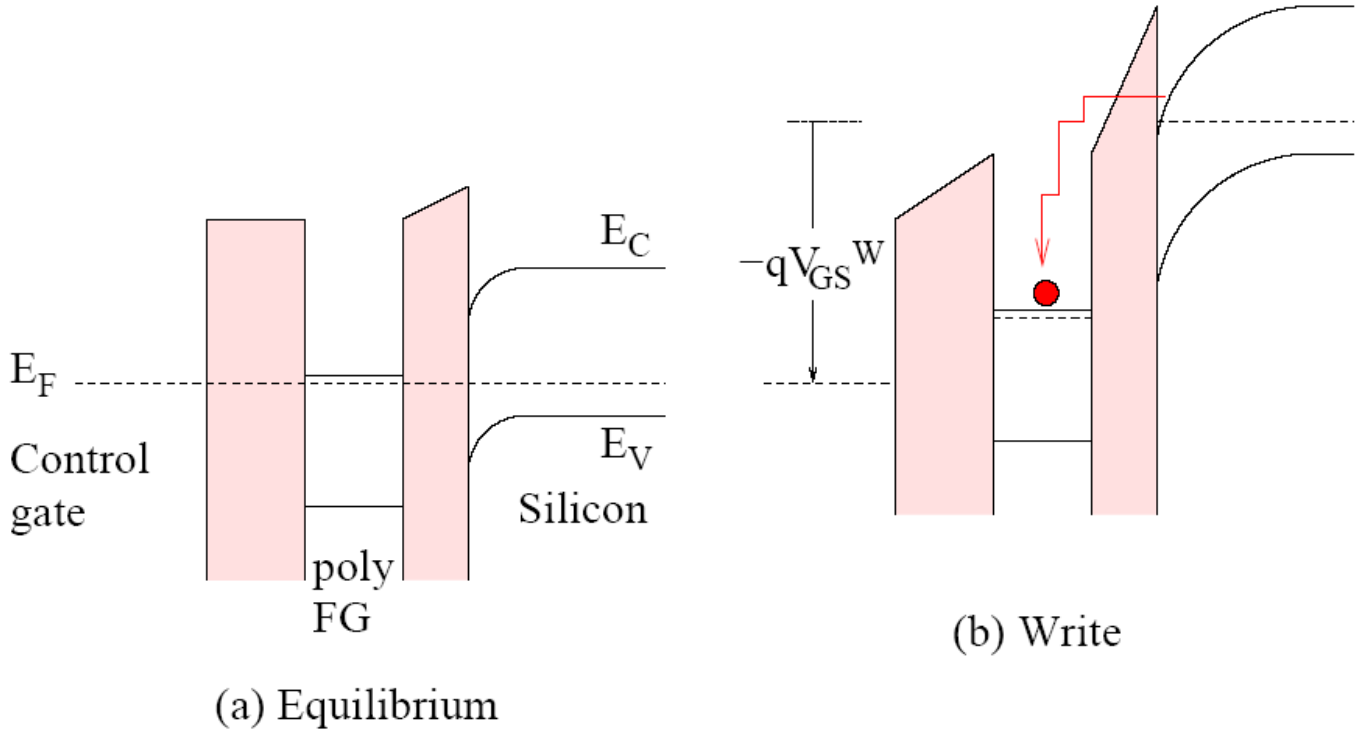
What is the difference in V_T in the two cases?

How is a ONE/ZERO interpreted?

Is the reading destructive?

Sec. 15.1

Writing a 0



$$T \approx \exp\left[-\frac{2d}{\hbar}\sqrt{2m_2^*(U_2 - E)}\right]$$

Where did this expression come from?

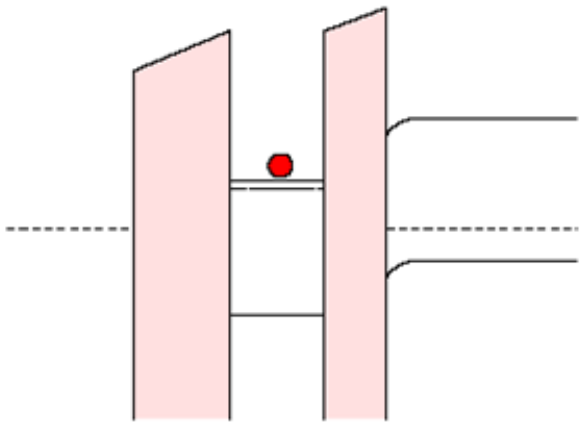
Both oxides are too thick for [ ]

Apply large [ ] voltage. This enables FAT.

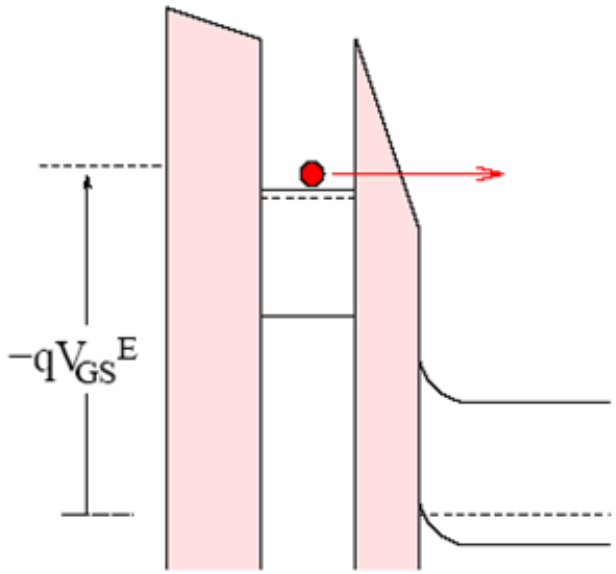
Electrons become trapped in the [ ]

Sec. 15.1

Storing, and Erasing a 0



(c) Store



(d) Erase

What happens to the stored charge if the power fails?

What's the polarity of the erase voltage?

http://www.toshiba.co.jp/about/press/2009_08/pr0401.htm

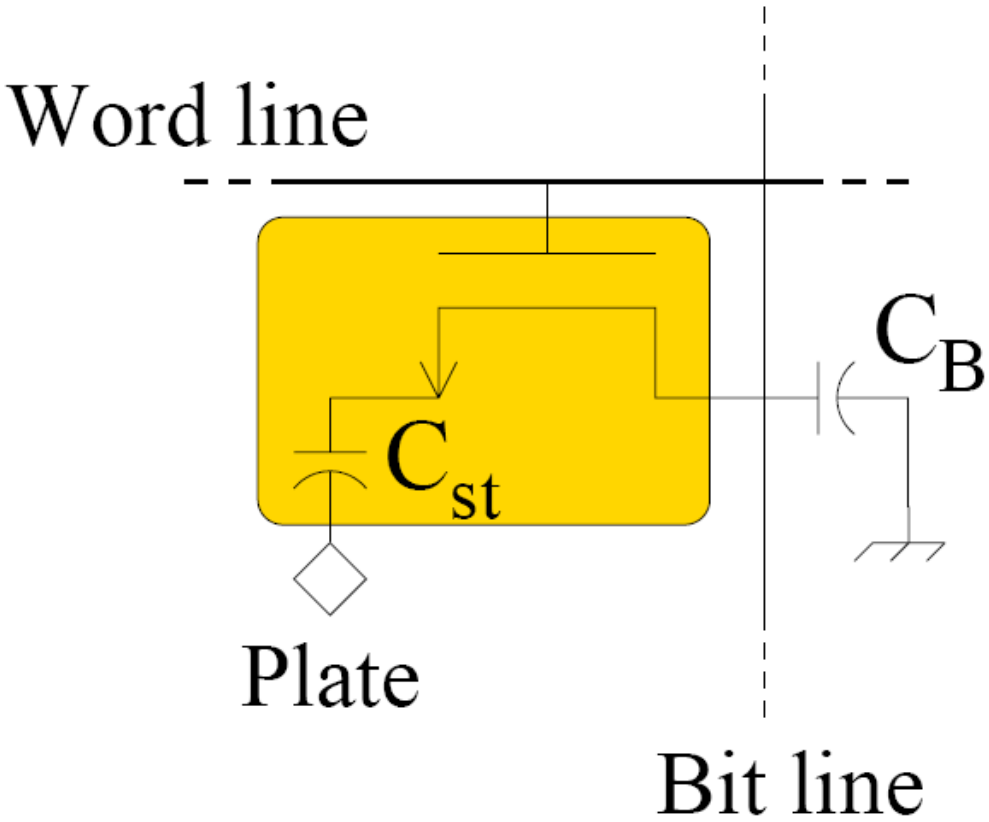
Toshiba to Launch the World's First SDXC Memory Card

World's largest 64gigabyte (GB), with world's fastest transfer rate

How has TOSHIBA done this?

Sec. 15.2

DRAM



Where is the charge stored?

What is the function of the MOSFET?

How is the cell read?

What is the condition of the bit-line during a READ operation?

Writing and Reading a ONE

WRITE:

Plate at VDD/2

Raise V_{Bit} to VDD+V_T

Enable word line.

What does V_S become?

What does V_{st} become?

READ:

Plate at VDD/2

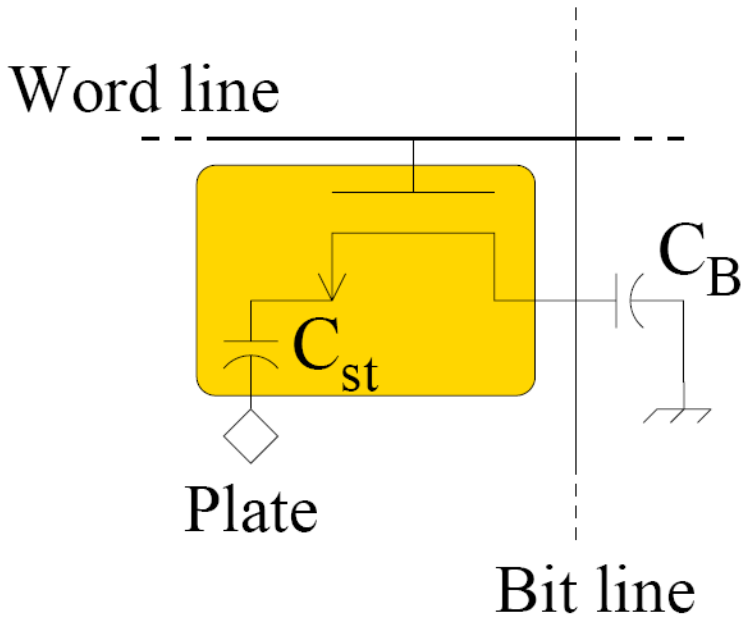
Pre-charge V_{Bit} to VDD/2

Float V_{Bit}

Enable word line

Sense V_{Bit}

What does V_{Bit} become?



Sec. 15.2

Writing and Reading a ZERO

WRITE:

Plate at VDD/2

What is V_{Bit} set to?

Enable word line.

What does V_S become?

What does V_{st} become?

READ:

Plate at VDD/2

Pre-charge V_{Bit} to VDD/2

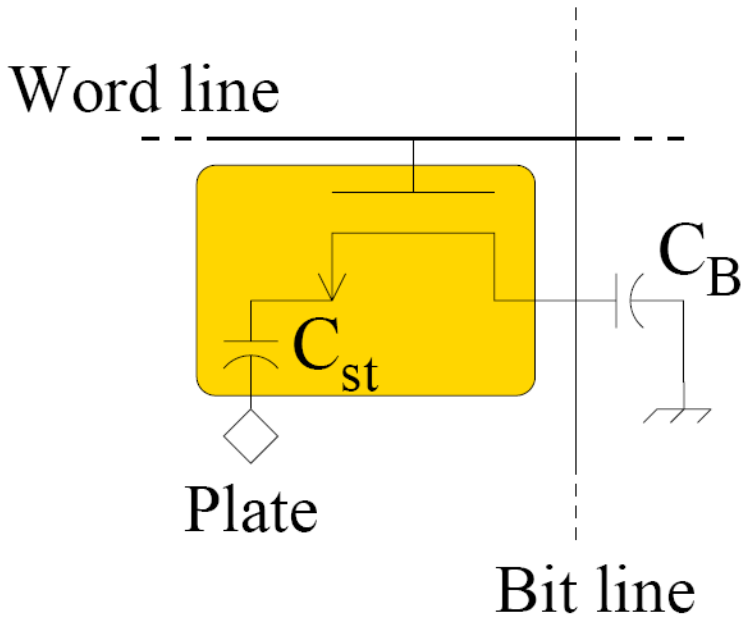
Float V_{Bit}

Enable word line

Sense V_{Bit}

What does V_{Bit} become?

Does V_S change?

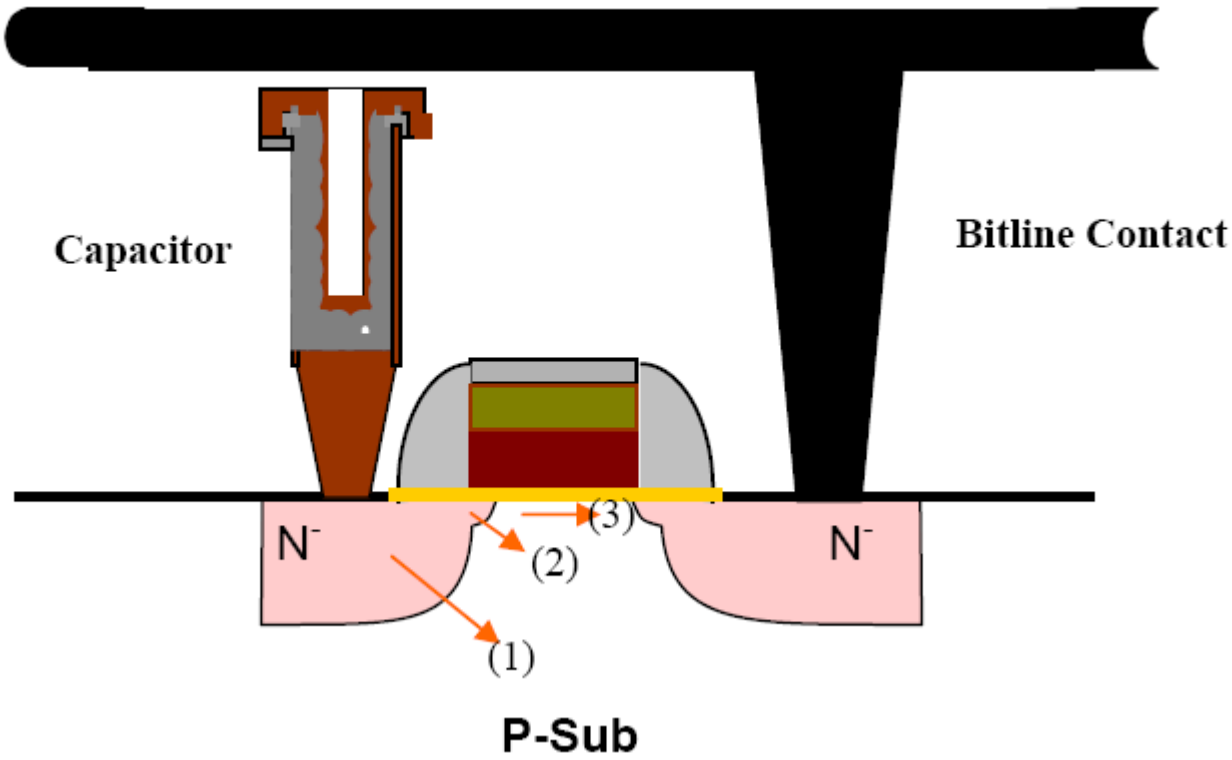


Why is this memory called “Dynamic”?

Sec. 13.1.10

Leakage currents

Another reason for frequent refreshing



(1) Reverse Junction leakage current from the storage node

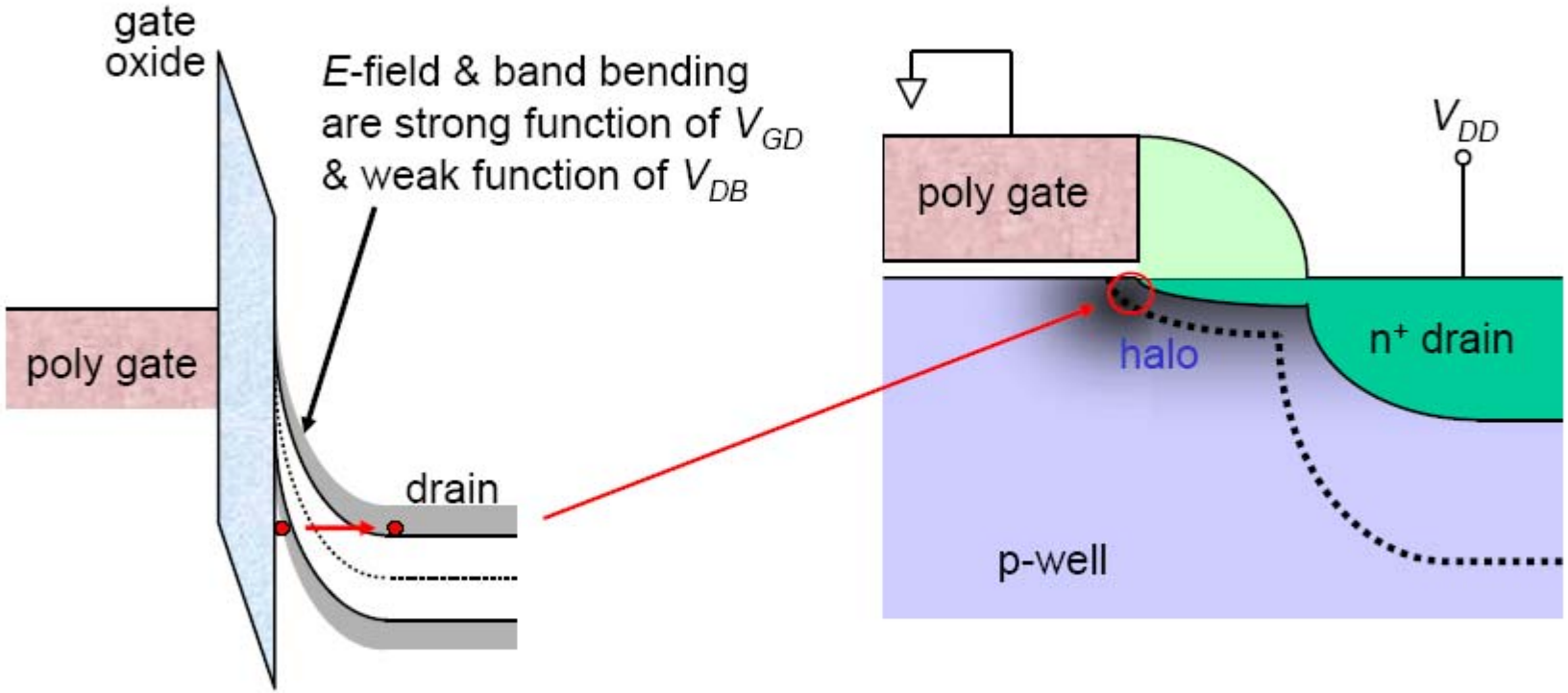
(2) Gate Induced drain leakage (GIDL) current

(3) Subthreshold leakage current of NMOS transistor

Sec. 13.1.10

Gate-Induced Drain Leakage (GIDL)

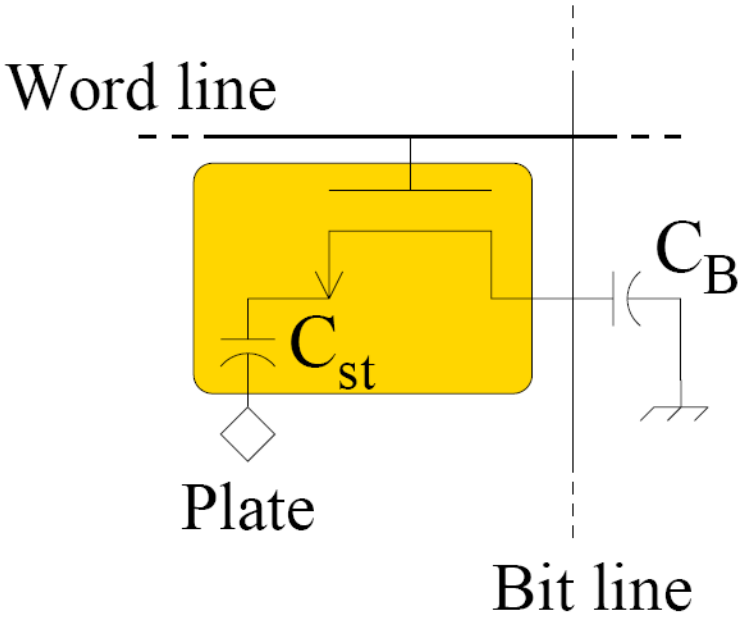
- Drain-to-substrate leakage due to band-to-band tunneling current in very high-field depletion region in drain overlap region



- Similar gate-induced source leakage (GISL) mechanism exists when source is raised above gate potential

Sec. 15.2

Charge sharing

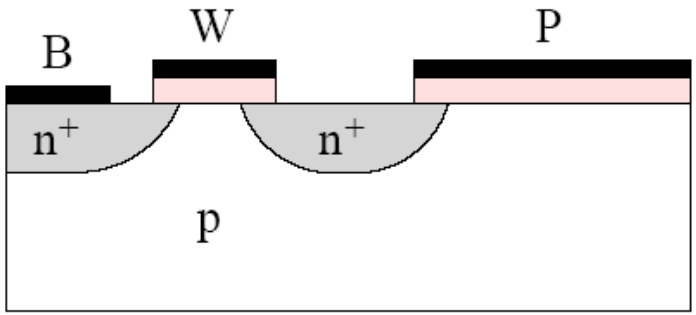


Basically, the DRAM works by altering the charge on the BIT line.

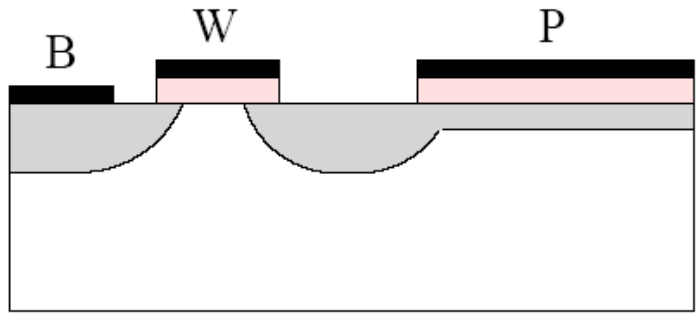
Therefore, is it required to make C_{st} as large or as small as possible?

Sec. 15.2

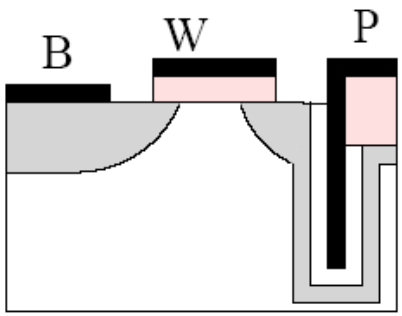
DRAM-capacitor evolution



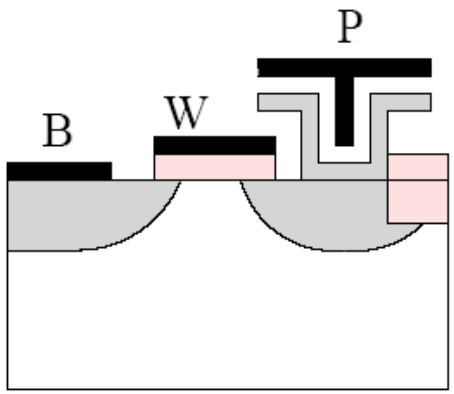
(a) MOS capacitor (4K)



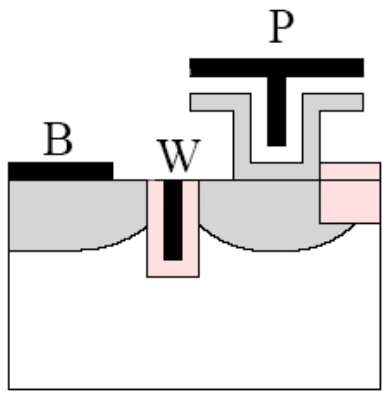
(b) Planar capacitor (64K – 1M)



(c) Trench capacitor (1M – 1G)



(d) Stacked capacitor (4M –)



(e) Buried word line (4G –)

480 reunion at the Hofbrauhaus