LECTURE 23

- memory organization
- memory-density trends
- flash memory
- DRAM
Industry strives to make cells as small as possible.

Identify:
- Memory cells
- Word lines
- Bit lines
- Decoder
- MUX/DEMUX

Sketch a MOST memory cell, showing word- and bit-line connections.
Memory Density

1965 Actual data and projection
MOS Arrays
MOS Logic 1975 actual data
1975 Projection
Memory
Microprocessor

Hans Moravec, CMU
What is the most significant difference from a regular MOSFET?

How is the cell programmed (written and erased)?

How is the cell read?
Let $Q_n = -4q$ represent inversion.

Enable word line.

Does the bit-line sense an $I_D$ in (a) and/or (b)?

What is the difference in $V_T$ in the two cases?

How is a ONE/ZERO interpreted?

Is the reading destructive?
Sec. 15.1

Writing a 0

Where did this expression come from?

Both oxides are too thick for direct tunneling. Apply large voltage. This enables FAT.

Electrons become trapped in the FG well.
Storing, and Erasing a 0

What happens to the stored charge if the power fails?

What’s the polarity of the erase voltage?
http://www.toshiba.co.jp/about/press/2009_08/pr0401.htm

**Toshiba to Launch the World's First SDXC Memory Card**  
World's largest 64gigabyte (GB), with world's fastest transfer rate

How has TOSHIBA done this?
Where is the charge stored?

What is the function of the MOSFET?

How is the cell read?

What is the condition of the bit-line during a READ operation?
Writing and Reading a ONE

WRITE:
Plate at VDD/2
Raise $V_{\text{Bit}}$ to VDD+$V_T$
Enable word line.
What does $V_S$ become?
What does $V_{st}$ become?

READ:
Plate at VDD/2
Pre-charge $V_{\text{Bit}}$ to VDD/2
Float $V_{\text{Bit}}$
Enable word line
Sense $V_{\text{Bit}}$
What does $V_{\text{Bit}}$ become?
Writing and Reading a ZERO

WRITE:
Plate at VDD/2
What is $V_{\text{Bit}}$ set to?
Enable word line.
What does $V_S$ become?
What does $V_{st}$ become?

READ:
Plate at VDD/2
Pre-charge $V_{\text{Bit}}$ to VDD/2
Float $V_{\text{Bit}}$
Enable word line
Sense $V_{\text{Bit}}$
What does $V_{\text{Bit}}$ become?
Does $V_S$ change?

Why is this memory called “Dynamic”?
Another reason for frequent refreshing

1. Reverse Junction leakage current from the storage node
2. Gate Induced drain leakage (GIDL) current
3. Subthreshold leakage current of NMOS transistor
Gate-Induced Drain Leakage (GIDL)

- Drain-to-substrate leakage due to band-to-band tunneling current in very high-field depletion region in drain overlap region

- Similar gate-induced source leakage (GISL) mechanism exists when source is raised above gate potential

Loke et al., 12-Mar-2008
Basically, the DRAM works by altering the charge on the BIT line.

Therefore, is it required to make $C_{st}$ as large or as small as possible?
Sec. 15.2

**DRAM-capacitor evolution**

(a) MOS capacitor (4K)

(b) Planar capacitor (64K – 1M)

(c) Trench capacitor (1M – 1G)

(d) Stacked capacitor (4M – )

(e) Buried word line (4G – )
480 reunion at the Hofbrauhaus