LECTURE 24

- revisiting the DRAM
- CMOS camera
- BJT logic
- ECL
- high-frequency performance comparison
WRITE:
Plate at VDD/2
Drive BIT to VDD
Raise $V_{\text{Word}}$ to VDD+$V_T$
What does $V_S$ become?
What does $V_{st}$ become?

READ:
Plate at VDD/2
Pre-charge $V_{\text{Bit}}$ to VDD/2
Float $V_{\text{Bit}}$
Enable word line
Sense $V_{\text{Bit}}$
What does $V_{\text{Bit}}$ become?
Does $V_S$ change?
Writing and Reading a ZERO

WRITE:
Plate at VDD/2
Drive BIT to 0.
Enable word line (VGS=VDD).
What does $V_S$ become?
What does $V_{st}$ become?

READ:
Plate at VDD/2
Pre-charge $V_{Bit}$ to VDD/2
Float $V_{Bit}$
Enable word line
Sense $V_{Bit}$
What does $V_{Bit}$ become?
Does $V_S$ change?

Why is this memory called “Dynamic”? 
Text: Bit-line voltage changes during READ

**Written-State**

\[ Q = C_s (V_{sn} - V_{cp}) + C_b V_{bl} \]

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“1”    \[ V_{sn} = V_{ccs} \]
“0”    \[ V_{sn} = 0 \]
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Precharge BL to \[ V_{bl} = V_{ccs} / 2 \]

Select WL with \[ V_{WL} > V_{ccs} + V_T^* \]

\[ Q = C_s (V'_{bl} - V_{cp}) + C_b V'_{bl} \]

\[ \Delta V = V'_{BL} - V_{BL} = (V_{SN} - V_{BL}) \frac{C_s}{C_s + C_b} \]

\[ \Delta V'_{1} = V'_{bl} - V_{bl} = \frac{1}{1 + C_b/C_s} \cdot \frac{V_{ccs}}{2} \]

\[ \Delta V'_{0} = V'_{bl} - V_{bl} = -\frac{1}{1 + C_b/C_s} \cdot \frac{V_{ccs}}{2} \]

What’s the point of \[ V_{plate} \]?

www.ece.ucsb.edu/bears/class/ece224a/Lecture12dram.ppt
Sec. 15.2

**DRAM-capacitor evolution**

(a) MOS capacitor (4K)  
(b) Planar capacitor (64K – 1M)

(c) Trench capacitor (1M – 1G)  
(d) Stacked capacitor (4M – )  
(e) Buried word line (4G – )
CMOS camera

\[ I_{\text{photo}} \quad I_{\text{dark}} \quad I_L \quad C_j \quad V_{\text{Load}} \]

\[ V_{\text{RST}} \quad V_{\text{DD}} \]

Row Decode

Column Decode
BJT Logic

Switching OFF from saturation:

Switching OFF from active:

Figure 11E.7 Determination of the dc operating point by the superposition of transistor characteristics and the load line. Three such points, for different base currents, are shown.
Figure 13.19 Large-signal equivalent circuit of the HBT. The collector current source is from Fig. 9.9.
Sec. 13.2

Why switching from saturation is slow

- Remove $V_{BE}$
- Depletion layers widen
- Holes flow OUT of base
- $i.e.$, $I_B$ is reversed
- $n(0)$ and $n(W_B)$ decrease as $V_j$'s decrease
- But $dn/dx$ stays same
- So $I_C$ stays same
- Until $n(W_B) = n_0$
Basics of ECL, a non-saturating logic

- R’s and biases chosen so that Q’s never saturate.
- Differential logic, so only a small swing in \( v_i \) needed for switching.
- \( \therefore \) ECL is very fast.

What are the drawbacks?

Figure 14.32. The basic element of ECL is the differential pair. Here, \( V_R \) is a reference voltage.

Figure 13.2. Examples of 2-input NOR gates. (a) in CMOS, (b) in HBT emitter-coupled logic (ECL). The latter has a higher transistor count because, in addition to the actual emitter-coupled switching element, level shifters and a current source are required. However, it should also be noted that the ECL gate shown does allow complementary outputs.
$f_T$ and $f_{\text{max}}$: HBT vs. MOS

$$2\pi f_T = \frac{g_m}{C_\pi + C_\mu (1 + g_m R_{cc})}$$

$$f_{\text{max}} = \sqrt{\frac{f_{T,i}}{8\pi C_\mu R_b}}$$

What are the corresponding expressions for MOSFETs?

Which is “better”, HBT or MOSFET?