Department of Electrical and Computer Engineering
UNIVERSITY OF BRITISH COLUMBIA

EECE 480 SEMICONDUCTOR DEVICES

FINAL EXAM, December 12, 2001

Time: 2.5 hours
Answer 4 (FOUR) questions.
All questions carry equal weight.
No notes, calculators or books allowed.
This exam consists of 2 pages

1. BJT

(a) Give precise definitions for f_T and f_{max} as they apply to bipolar transistors.

(b) Identify the various device features that determine f_T and f_{max}, and comment on their relative importance.

(c) Discuss how vertical shrinking and lateral shrinking of a BJT affect f_T and f_{max}.

2. HBT

Consider an *n-p-n* HBT which has emitter and collector regions made from material A and base region made from material B. Material A has an electron affinity of 3 eV and a bandgap of 5 eV; the corresponding, respective quantities for material B are 4 eV and 2 eV. The emitter doping density is higher than that of the collector.
(a) Construct the equilibrium energy band diagram, roughly to scale, of the HBT, showing the vacuum level, the conduction- and valence- band edges, and the Fermi level.

(b) Discuss how the current gain β of the above HBT would change if the following changes were made separately:
(i) the collector material was replaced by material B (doping density unchanged);
(ii) the base material was replaced by material A (doping density unchanged).

3. HFET

(a) Discuss the structure and operation of MESFETs and MODFETs.

(b) What advantages do these transistors offer over Si MOSFETs?

(c) Explain, with the aid of energy band diagrams:
(i) how a given metal/semiconductor contact may be either rectifying or ohmic;
(ii) how MESFETs can take the form of either enhancement or depletion devices.

4. MOSFET

(a) How does the prediction of the LEVEL 1 SPICE model for the drain current compare with the measured value? What is the reason for the discrepancy?

(b) Sketch a plot of $I_{D,sat}$ versus channel length L for the following 3 models:
(i) when current saturation is predicted to occur due to channel pinch-off;
(ii) when the full velocity-field relationship for electrons is considered;
(iii) when current saturation is due solely to velocity saturation, and the channel length is very short.

Discuss the reasons for the differences between the 3 curves on your plot, and comment on the implications for accurate prediction of $I_{D,sat}$ in short-channel devices.

(c) Generally, how and why does $V_{DS,sat}$ change as L shrinks?

5. CMOS

(a) Regarding the operation of deep sub-micron CMOS inverters, discuss the factors affecting:
(i) switching speed;
(ii) standby power dissipation;
(iii) dynamic power dissipation.

(b) Graphically represent the above three phenomena in the $V_T - V_{DD}$ plane, and comment on the allowable design space for high-performance devices.