Department of Electrical and Computer Engineering
UNIVERSITY OF BRITISH COLUMBIA

EECE 480 MICROELECTRONIC DEVICES

FINAL EXAM, December 06, 2006

Time: 2.5 hours
ANSWER ALL QUESTIONS.
All questions carry equal weight.
No notes, programmable calculators or books allowed.
This exam consists of 2 pages.

1.
(a) Consider a metal/AlGaAs/GaAs HEMT with no spacer layer. The workfunctions of the metal, AlGaAs and GaAs can be taken as 3.5, 2, and 4 eV, respectively. The electron affinities of the AlGaAs and GaAs are 1.5 and 3 eV, respectively. The bandgaps of the AlGaAs and GaAs are 4 and 2 eV, respectively.
Draw energy band diagrams, showing to approximate scale in energy (*e.g.*, 1 line spacing $\equiv$ 1 eV), the zero-field- and local-vacuum levels, the conduction bands and valence bands for the two semiconductors, and the Fermi levels for the metal and the semiconductors:
(i) for the three, separated components of the device;
(ii) for the joined components at equilibrium.
(b) For the HEMT in the above question:
(i) What is the height of the Schottky barrier?
(ii) What is the height of the potential well at the AlGaAs/GaAs interface?
(iii) Why do the electrons in the channel populate sub-bands, rather than a single conduction band?
(c) HEMT#A and HEMT#B are identical, except that $\Phi_{\text{gate,A}} < \Phi_{\text{gate,B}}$, where Φ is the metal workfunction. Which transistor has the more negative threshold voltage, and why?

2.
(a) Consider two HBTs, HBT#X and HBT#Y, which are identical, except that HBT#X has 2 base contacts (one either side of the emitter finger), whereas HBT#Y has only one base contact. Which HBT would have the better noise figure at very high frequencies? Give the reasons for your answer.
(b) Sketch the $I_C - V_{CE}$ characteristic of an IGBT. How and why is the magnitude of the forward breakdown voltage different from that of the reverse breakdown voltage?
(c) Consider two diodes: one is a metal/n-Si Schottky diode, and the other is a p^-/n-Si homojunction. The n-type doping is quite high and is the same for both diodes. Which diode is more likely to deliver a forward-bias electron current at the hemi-Maxwellian velocity limit? Give reasons for your answer.

3.

(a) Sketch the cross-section of a DRAM cell, clearly identifying the BIT-, WORD-, and PLATE-electrodes, and the channel-stop diffusion.

(b) *(i)* Sketch the surface potential profile ($\psi_s(x)$) in the silicon body under each of the 3 electrodes immediately after a ONE has been written.

(ii) Why is this condition unstable?

(iii) What would be the biases (either HI or LO) on the 3 electrodes when writing a ZERO? Explain the reasons for your choices.

(c) A Flash Memory cell has a top insulator (between the control gate and the floating gate) of thickness 200 nm. The bottom insulator thickness is 10 nm. Each insulator has a permittivity of 32×10^{-12} F/m. A stored ONE is able to be read with $V_{GS} = 1$ V.

For the same V_{GS}, will there be a change in bit-line potential when reading a ZERO, *i.e.*, when there are 10^{10} electrons/cm^2 on the floating gate? Support your answer with a numerical calculation.

4.

(a) Give two reasons why it is important to have a high capacitance per unit area for the gate oxide in Si MOSFETs intended for ULSI digital applications.

(b) Why is there an urgency to find a replacement for SiO_2 as the gate dielectric for advanced CMOS FETs?

(c) In CMOS90, C_{ox} can be taken as $2\epsilon_0$ F/m^2, and the electron affinity of the semiconductor Si can be taken as 4 eV. Two dielectrics, Oxide#P and Oxide#Q, are being considered as replacement gate oxides to double C_{ox}. The electron affinity and relative permittivity for Oxide#P are 1 eV and 8, respectively, whereas the corresponding values for Oxide#Q are 4 eV and 16. Which is the more suitable dielectric, and why?

5.

(a) Discuss the advantages and disadvantages of continuing to reduce the gate length of Si MOSFETs.

(b) Explain how the electron mobility in Si can be increased by strain.

(b) Consider a typical CMOS90 Si N-MOSFET with $V_{DS} = 1$ V. Estimate the ratio g_m/I_D at two gate-source biases: *(i)* $V_{GS} = (V_T - 0.5)$ V, and *(ii)* $V_{GS} = (V_T + 0.5)$ V. Comment on the reasons for any difference between the two estimates.