Department of Electrical and Computer Engineering
UNIVERSITY OF BRITISH COLUMBIA

EECE 480 MICROELECTRONIC DEVICES

FINAL EXAM, December 5, 2008

Time: 3 hours
ALL QUESTIONS MAY BE ATTEMPTED. A mark of greater than 50/50 is possible.
Notes and non-programmable calculators are allowed.
Programmable calculators, telecommunications devices and computers are NOT allowed.
This exam consists of 3 pages.

Information on CMOS90 technology:
$V_{DD} = 1.0\,\text{V}$;
$L = 90\,\text{nm}$;
$t_{ox} = 2.3\,\text{nm}$;
$\epsilon_{ox} = 3.9\epsilon_0$;
$N_A = 8.3 \times 10^{17}\,\text{cm}^{-3}$;
$\mu_{\text{eff}} = 230\,\text{cm}^2(\text{Vs})^{-1}$;
$v_{sat} = 7 \times 10^6\,\text{cm/s}$.

Information on CMOS65 technology:
$V_{DD} = 1.0\,\text{V}$;
$L = 65\,\text{nm}$;
$t_{ox} = 1.7\,\text{nm}$;
$\epsilon_{ox} = 3.9\epsilon_0$;
$N_A = 2.6 \times 10^{18}\,\text{cm}^{-3}$;
$\mu_{\text{eff}} = 600\,\text{cm}^2(\text{Vs})^{-1}$;
$v_{sat} = 9 \times 10^6\,\text{cm/s}$.

Other information:
$\chi = 4.1\,\text{eV}$ for Si; $\epsilon_r = 11.9$ for Si; $\chi = 4.07\,\text{eV}$ for GaAs.
$h = 6.63 \times 10^{-34}\,\text{Js}$; $k_BT = 0.0259\,\text{eV}$; $q = 1.6 \times 10^{-19}\,\text{C}$; $\epsilon_0 = 8.85 \times 10^{-12}\,\text{F/m}$; $m_0 = 9.11 \times 10^{-31}\,\text{kg}$.

1. [12 marks]

(a) Over the last few decades, the trend in Si MOSFETs has been to reduce the gate length, the oxide thickness, and the source/drain-junction depth, and to increase the body doping density.
Explain why each of these four parameters has been systematically changed.

(b) In recent years, the trend has been for the 'long-channel threshold voltage' to increase, *e.g.*, for CMOS90 N-FETs V_{T0} is about 0.25 V, whereas it is about 0.4 V for CMOS65 N-FETs.
Why (not how) is V_{T0} being deliberately designed to be higher as CMOS technology evolves in the modern era?

(c) The parameters for CMOS45 are not yet well known, but one might expect a thicker high-k dielectric for the gate oxide, *e.g.*, $\epsilon_r = 16$ and $t_{ox} = 8\,\text{nm}$, a metal gate, and perhaps a slightly reduced doping density in the body, *e.g.*, $1 \times 10^{18}\,\text{cm}^{-3}$.
If the target value for V_{T0} is 0.45 V, what must be the workfunction of the metal gate?

2. [12 marks]

(a) Prior to developing the surface-potential model for a FET it is necessary to establish a relationship between the electron concentration in the y-direction and the potential $\psi(y)$.
Equation (12.4) is supposed to be such a relation, but the right-most version of it is incorrect.
Correct the mistake in the equation.

(b) Tensile strain can improve the electron mobility in Si N-FETs by lowering the energy of the Δ_2 valleys with respect to the Δ_4 valleys (see Fig. 13.5).
If a particular stress results in 80% of the electrons residing in the Δ_2 valleys, estimate the percentage improvement in electron mobility with respect to the unstrained case.

(c) For a CMOS65 N-FET the band bending in the semiconductor is steep enough that the potential-energy profile near the silicon/oxide interface can be approximated as a rectangular potential well of infinite height.
All the electrons can be taken as residing in the first energy subband (see Fig. 16.11), which is located 0.377 eV above the conduction-band edge. The electron effective mass can be taken as m_0.
Estimate the percentage change in effective oxide capacitance due to consideration of this electron confinement.

3. [12 marks]

(a) Consider an HBT with a single emitter contact of lateral width h and a single base contact. There is a power dissipation P_B in the base due to the presence of a base current I_B and a base-spreading resistance $R_{B,sp}$.
The emitter is now divided into two emitters, each of lateral width $h/2$, and the base current is now split between three base contacts that are interdigitated with the emitter fingers as shown in Fig. 17.3b.
What improvement in base power dissipation P_B is achieved by using this interdigitated structure rather than the single-emitter/single-base arrangement?

(b) Consider an *Npn* $In_{0.51}Ga_{0.49}P$/GaAs/GaAs HBT operating in the active mode with $V_{BE} = 1.25\,V$ and $V_{BC} = -3.0\,V$. The emitter doping density is $10^{18}\,cm^{-3}$ and the width of the emitter quasi-neutral region is 100 nm. The corresponding values for the base are $10^{19}\,cm^{-3}$ and 25 nm. The cross-sectional area of the HBT is $(1 \times 1)\,mm^2$. The minority carrier properties of the InGaP can be taken to be the same as for correspondingly doped GaAs. (This is the same device as used in Assignment 4. You can use the results of any calculations performed for that assignment if you wish).
Estimate the transconductance and the input conductance of the HBT under the stated operating conditions.
Clearly state any assumptions that you make to get the estimates of these small-signal parameters.

(c) For the HBT used to generate Fig. 11.6, it appears that the current gain (h_{21}) flattens out at 'low' frequencies, *i.e.*, below about 3 GHz.
By examining the development of the expression for the current gain in section 11.3.1, derive an expression for the frequency-independent, low-frequency current gain $|i_c/i_b|^2$ in terms of two of the small-signal parameters for the transistor.

4. [12 marks]

(a) Fig. 8.4 shows the band diagram for a P^+pN^+ AlGaAs/GaAs/AlGaAs LED under forward bias.
Construct the corresponding band diagram for an $In_{0.51}Ga_{0.49}P/GaAs/In_{0.51}Ga_{0.49}P$ LED.
Show the development of your band diagram, and try and keep your diagrams to an approximately correct vertical scale. Show E_0, E_l, E_C, E_V and, where appropriate, E_F.

(b) Explain which of the above two LEDS (the AlGaAs device or the InGaP device) is likely to have the better current efficiency.

(c) Two LEDS, A and B, each emit 1 mW of optical power when operating at a current of 1 mA and a forward bias of 2 V.
LED A emits in the ultra-violet part of the spectrum, and LED B emits at 470 nm in the blue part of the spectrum. For each diode evaluate:

(i) the wall-plug efficiency;

(ii) the luminous efficacy;

(iii) the luminous efficiency.

5. [12 marks]

(a) A floating-gate flash memory cell of the construction shown in Fig. 15.1 uses a word-line voltage of 1.5 V during the READ operation. The upper insulator is silicon dioxide and has a thickness of 20 nm. The threshold voltage when there is no charge stored on the floating gate is 1.0 V. The area of the floating gate is $(100 \times 100\,)\text{nm}^2$.
How many electrons need to be stored on the floating gate to represent a ZERO?

(b) Consider a stacked-capacitor DRAM with its storage capacitor of 1 pF charged to 1 V. This represents a stored ONE.
The FET in the DRAM is a CMOS65 N-FET of width $Z = 100$ nm.
If charge leakage from the storage capacitor is due to the sub-threshold current of the FET, how long will it take for the storage capacitor to lose 50% of its charge?
You may use the results of any calculations from Assignment 5 if you wish.

(c) Consider Fig. 16.14b, c, and d. This sequence shows an HJFET at equilibrium, with a small negative gate voltage applied, and with a gate voltage equal to the threshold voltage, respectively. Call this HJFET A.

(i) Draw a similar sequence of partial band diagrams (E_C and E_F and + charges) for an HJFET with a thicker barrier layer, *i.e.*, one that is not fully depleted at zero bias, as in Fig. 16.14a. Call this HJFET B.

(ii) Which of the two HJFETs has the more positive threshold voltage? Give your reasoning.