Department of Electrical and Computer Engineering
UNIVERSITY OF BRITISH COLUMBIA

EECE 480 Semiconductor Devices: Physics, Design and Analysis.

FINAL EXAM, December 19, 2009

Time: 3 hours
ALL QUESTIONS MAY BE ATTEMPTED. A mark of greater than 50/50 is possible.
Notes and non-programmable calculators are allowed.
Programmable calculators, telecommunications devices and computers are NOT allowed.
This exam consists of 2 pages.

1. [12 marks]

(a) One of the features of scaling in high-performance Si MOSFETs has been the progressive increase in the substrate doping density. What is the reason for this?

(b) What is the purpose of halo doping?

(c) Fig. 13.3 shows the effect of doubling μ_{eff} on the drain characteristic of a high-performance Si N-FET. Why does the saturation current not increase by a factor of 2?

(d) Consider CMOS90 and CMOS65 N-FETs operating in the subthreshold regime. Determine which transistor would need the smaller gate-source voltage swing to reduce its drain current by a factor of 10.

(e) One exciting prospect for future high-performance Si ICs is the possibility of having FETs with different threshold voltages on the same chip. This could be achieved by depositing different metals for the gates of transistors in different parts of the chip. Two metals being considered are titanium and nickel, for which the work functions are 4.33 and 5.01 eV, respectively.
If this scheme were implemented for CMOS65 N-FETs, which transistors (Ti or Ni gates) would have the higher threshold voltage?

2. [12 marks]

(a) Fig. 15.4b shows the energy band diagram of a Flash memory cell during the writing of a ZERO. Draw the corresponding energy band diagram for the case of writing a ONE.

(b) Consider the storage mode of operation in a Flash memory comprising n^+ polysilicon gates and silicon dioxide insulators. The electrons stored on the floating gate can be considered to all have a kinetic energy of $3k_BT/2$.
Simplify the tunneling barrier, and then determine an estimate of how thick the top oxide must be if the tunneling probability between the gates at this energy is to be $\approx 10^{-30}$.

(c) Consider a stacked-capacitor DRAM with a storage-node capacitance of 1 pF. The plate electrode is held at $V_{DD}/2$, and this is also the voltage to which the bit-line is pre-charged. $V_{DD} = 1\,\text{V}$. The bit-line sensing circuitry can detect a voltage change of 10 mV, and this is used to distinguish between a stored ONE and a stored ZERO in a single cell.
Compute the magnitude of the bit-line capacitance.

3. [12 marks]

An AlGaAs/p-GaAs/AlGaAs LED of the type shown in Fig. 8.2 has a p-GaAs region of doping density $10^{15}\,\mathrm{cm}^{-3}$. The diode operates at a forward bias of 1.25 V and a current of 1 mA; this induces high-level injection conditions in the active (p-GaAs) layer, resulting in an excess minority carrier concentration of $10^{19}\,\mathrm{cm}^{-3}$. 90% of the recombination occurs in the active layer, and 50% of the light generated within the device is emitted through the desired surface.

(a) Evaluate the wall-plug efficiency.

(b) Evaluate the luminous efficiency.

4. [12 marks]

(a) Consider a Si n^+p diode in which the quasi-neutral base region W_B is much, much, much longer than the electron minority carrier diffusion length L_e, and the quasi-neutral emitter length W_E is much, much, much shorter than the hole minority carrier diffusion length L_h. The contacts at each end of the diode are ohmic.

Derive an expression for the diode saturation current I_0 in terms of the relevant lengths and minority carrier properties.

(b) The above diode is made into a solar cell with doping densities in the emitter and base of 10^{19} and $10^{16}\,\mathrm{cm}^{-3}$, respectively; $W_E = 100\,\mathrm{nm}$ and $W_B = 500\,\mu\mathrm{m}$. The area of the junction is $100\,\mathrm{cm}^2$.

Evaluate I_0.

(c) Under AM1.5G sunlight the cell gives a photocurrent of 4 A and a photovoltaic conversion efficiency of 20 %. The parasitic series and shunt resistances are negligible.

Evaluate: **(i)** the open-circuit voltage; **(ii)** the fill-factor.

5. [12 marks]

(a) Consider an HBT of the construction shown in Figure 14.5. What is the purpose of having a two-part collector?

(b) Consider a specific *Npn* $\mathrm{In_{0.51}Ga_{0.49}P}$/GaAs/GaAs HBT with a base and a sub-collector that are very highly doped. The lightly doped collector is $2\,\mu\mathrm{m}$ wide (vertical dimension) and has a doping density of $10^{16}\,\mathrm{cm}^{-3}$.

(i) Estimate the base-collector voltage at which the lightly doped collector becomes fully depleted.

(ii) When the transistor is operating at the V_{BC} just calculated, does the base-collector junction breakdown (see Table 16.1)?

(c) Determine whether f_T for an HBT of the construction in Fig. 14.5 would increase or decrease if every feature of the device was reduced in both of its lateral (horizontal) dimensions by a factor of 2.