Lecture 7

Noise Margin in Digital Circuits

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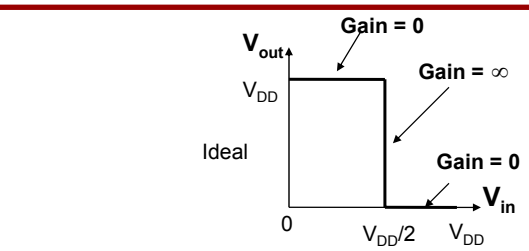
Overview

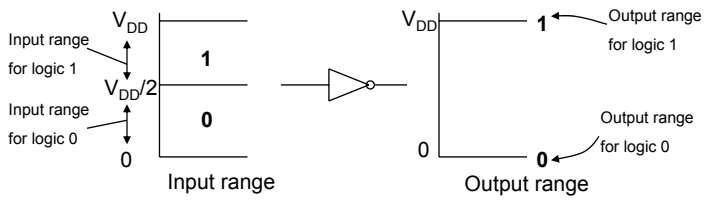
- **Reading**
  - HJS Chapter 4; Sections 4.1, 4.2, 4.3
- **Background**
  - Digital IC designs must operate properly in noisy environments. We would like to have some notion of how robust a circuit is to external noise sources. There are a variety of measures of noise for logic circuits such as single stage noise margin (SSNM) and the classical noise margins are based on the unity gain points of the VTC. These metrics eventually lead us to desirable properties that logic gates must have in order to work properly. We will look at how to calculate this for inverters in the next lecture.

Noise Margins and Sensitivity

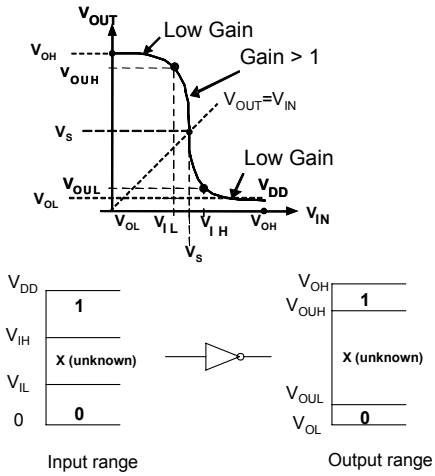
- Robustness of a circuit (i.e., its ability to operate properly in the presence of noise) depends on two factors:
  1. Noise margins (voltage metric)
     - how much noise can we apply before the gate fails
     - many different ways to measure this
  2. Noise sensitivity
     - how much noise can actually couple into the gate
     - depends on gate type and its connection to noise source
- First component sets requirements on the gate to handle noise
- Second component captures the response of the circuit to a given noise input (will be discussed in later chapters of HJS)
- Start by examining the first issue using basic inverter circuit…

Ideal Inverter Characteristics



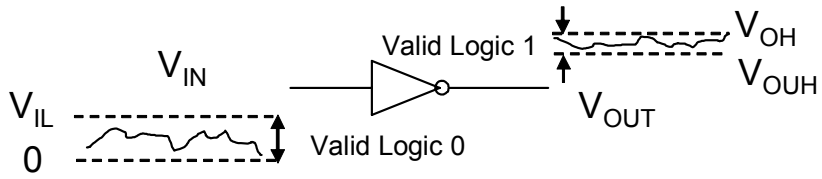


Actual Inverter Characteristics



Noise Attenuation

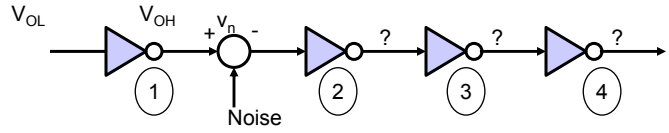
- What does this type of VTC imply about a noisy signal as it passes through a logic gate?
- Noise is reduced:



- Next, consider metrics for noise tolerance and the implications on the characteristics of the gate

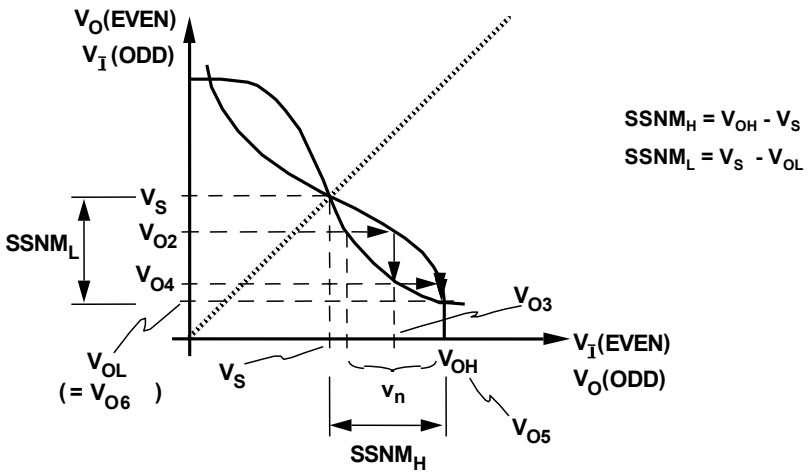
Single Stage Noise Margins

- Simplest type of noise margin is the single-stage noise margin
- Defined as maximum noise, v_n, in a single stage that still allows subsequent stages to recover to the right value (regenerative property)



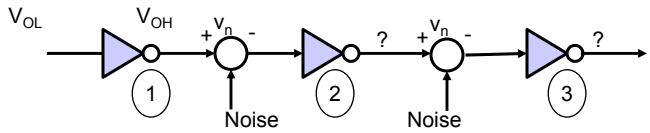
- In the above circuit $V_{i2} = V_{o1} - v_n = V_{OH} - v_n$
- For noise added to a high level input, the correct levels will be maintained if $V_{OH} - v_n > V_{TH}$ (point where $V_{in} = V_o$)
- For noise added to a low level input, correct levels will be maintained if $V_{OL} + v_n < V_{TH}$

Single Stage Noise Margins



Multistage Noise Margins

- Noise actually occurs between every gate and not at a single stage, as we have assumed so far

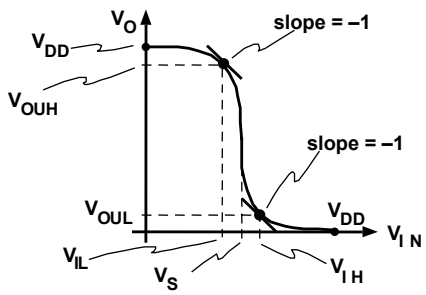


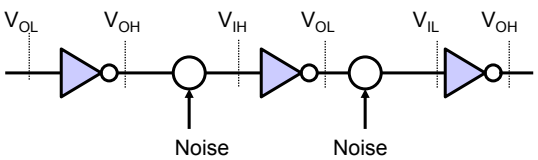
- In the above circuit, we need to determine how much noise we can tolerate before the circuit stops working as expected
- We note that Vout = f(Vin)
- With noise Vout' = f(Vin) + Vnoise x Gain + Higher-order terms
- If the Gain < 1, then noise is attenuated; otherwise it is amplified
- IDEA: Develop a metric based on keeping the Gain < 1

Classical Noise Margins

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$



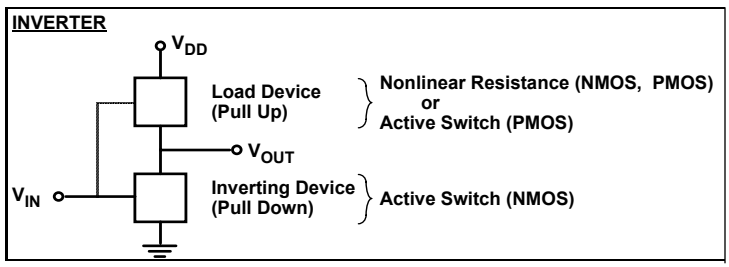


Requirements for a Valid Logic Gate

- Must have a high gain region between two low gain regions
- Gain must be below 1 for low gain regions
- Gain must be greater than 1 for high gain region
- Output must swing from valid low to valid high
  - Low output should be below V_{IL}
  - High output should be above V_{IH}

Next lecture: MOS Inverters

- Basic structure of MOS inverter is shown below: NMOS pulldown device with a variety of possible pullup devices



- We will derive the noise margin parameters for different types of inverters