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Extrapolated $f_{\text{max}}$ for carbon nanotube field-effect transistors

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1. Introduction

The frequency $f_{\text{max}}$, at which the extrapolated power gain becomes unity, is a well established figure of merit for characterizing the high-frequency performance of transistors. A useful, compact expression for $f_{\text{max}}$ is available for heterojunction bipolar transistors [1], but, in Si metal–oxide–semiconductor field-effect transistors, the need to consider the electrical properties of the substrate makes for a more complicated situation. However, in carbon nanotube field-effect transistors (CNFETs), the substrate is not an active part of the device, so the traditional, small-signal equivalent circuit, in which there are no elements representing the substrate [2, p 441], can be used as a basis for deriving a useful expression for $f_{\text{max}}$. Moreover, because of the small size of CNFETs, the quasi-static approximation should be valid up to very high frequencies. Here, starting from the small-signal parameters of the equivalent circuit, we systematically make a series of approximations that lead to compact expressions for the extrapolated $f_{\text{max}}$. These expressions are shown to be applicable over a wide range of conditions, and to be useful in guiding the design of high-frequency devices.

2. Modelling procedures

The small-signal, extrinsic $z$-parameters for the equivalent circuit shown in figure 1 are given by the standard expressions [2, p 440]

\[
\begin{align*}
 z_{11e} & = y_{22}/Y + R_{eg} \\
 z_{12e} & = -y_{12}/Y + R_s \\
 z_{21e} & = -y_{21}/Y + R_s \\
 z_{22e} & = y_{11}/Y + R_{ed} \\
 Y & = y_{11}y_{22} - y_{12}y_{21},
\end{align*}
\]

where $R_{eg} = R_i + R_g$, $R_{ed} = R_i + R_d$, and the intrinsic $y$-parameters are [3, p 378]

\[
\begin{align*}
y_{11} & = j\omega(C_{gs} + C_{gd}) \\
y_{12} & = -j\omega C_{gd} \\
y_{21} & = g_m - j\omega(C_m + C_{gd}) \\
y_{22} & = g_m + j\omega(C_m + C_{gd}).
\end{align*}
\]

The transcapacitance $C_m$ relates non-reciprocal capacitance in the extricated unit-current-gain frequencies are that the frequency at which the gain rolls off at $-10$ dB/decade, follows, namely [2, p 441]

\[
\frac{1}{\omega_t} = \frac{1}{\omega_1} [1 + g_{m} R_d] + R_{ed} C_{gd},
\]

where the intrinsic ‘cut-off’ frequency is given by

\[
\omega_1 = \frac{g_m}{(C_{gs} + C_{gd})}.
\]

The assumptions made in arriving at the expressions for the extrapolated unit-current-gain frequencies are that the frequency at which the extrapolation can properly begin is subject to the following restrictions:

\[
\begin{align*}
\omega^2 & \ll \frac{g_m^2}{(C_m + C_{gd})^2} \\
\omega^2 & \ll \frac{g_m}{(AR_{ed})} \\
\omega^2 & \ll \frac{g_m^2}{(C_{dd} + BR_d)^2} \\
\omega^2 & \ll \frac{(C_{dd} + BR_d)^2}{(AR_{ed})^2},
\end{align*}
\]
To make progress in simplifying equation (14), one has to compare component values, which, because of their bias and device dependence, cannot be expected to result in relations that are as generally applicable as the frequency limitations stated earlier in equations (5)–(8) and (10). We start by asserting

$$C_{gs} = C_{gd}.$$  \hspace{1cm} (15)

The motivations for doing this are the small size and longitudinal symmetry of CNFETs: the electrodes are inevitably very close together, so the extrinsic contributions to $C_{gs}$ and $C_{gd}$ will be significant; and the symmetry would make them equal. We can anticipate this equality breaking down at low and high gate bias, when the electrode-dependent quantum-capacitance contribution to $C_{gs}$ and $C_{gd}$, respectively, is particularly significant [5]. Using equation (15) in (14) leads to a considerable simplification:

$$\tau_{\text{eff},2}^2 = \frac{C_{gd}^2}{g_m} \left(1 + \frac{2g_{ds}}{g_m}\right) \frac{2R_g + R_c}{1 + R_c} \left[g_m + 2g_{ds}\right].$$  \hspace{1cm} (16)

Finally, in the interests of further simplification, we suggest $g_m \gg 2g_{ds}$. \hspace{1cm} (17)

This inequality may break down in CNFETs with small-diameter (large-bandgap) nanotubes, for which the transconductance is generally less than in those with large-diameter tubes. The result of this additional assumption is a very compact expression:

$$\tau_{\text{eff},3}^2 = \frac{C_{gd}^2}{g_m} \frac{2R_g + R_c}{1 + R_c} (1 + g_m R_c).$$  \hspace{1cm} (18)

In the next section we evaluate the validity of equations (14), (16) and (18) for several Schottky-barrier CNFETs. The component values are evaluated as described previously [5], using a Schrödinger–Poisson solver [6], with the inclusion of the complex band structure of the nanotube [7]. We found that it was not necessary to consider more than the lowest, doubly degenerate band for the tubes and bias ranges considered in this work.

3. Results and discussion

In seeking ultimate performance limits we examine devices of the coaxial structure shown in figure 2, but we base values for the physical properties on those of currently realizable planar structures, such as a recent, high-DC-performance device [8]. All the devices considered here have a gate of length $L_g = 50$ nm and of thickness $t_e = 20$ nm, an insulator relative permittivity of 16 (HfO$_2$), and Pd end-contacts of radius $t_c = 4$ nm. Unless otherwise stated, the contact length is $L_c = 100$ nm, the gate underlaps are $L_{uL} = L_{uR} = 5$ nm, and the contact resistances are computed from a Pd resistivity of 0.48 kΩ, which can be inferred from [8]. The data of [9] were used for the tube-dependent, end-contact barrier heights, while the work function of the gate was set equal to that of the nanotube [10]. The latter assignment is arbitrary in view of the lack of information on other factors, such as oxide charge, that will affect the threshold voltage in practice, and serves only to change the effective gate potential. The gate

$$\tau_{\text{eff},1}^2 = \frac{B}{8} \left\{ R_g \left[C_{dd} + B g_{ds} + A \right] \frac{g_{dd}}{g_m} \right\},$$  \hspace{1cm} (19)

where, for convenience, we have assumed similar source and drain contacts, and set $R_s = R_d = R_c$.\hspace{1cm}
It can be seen that the lowest \( \tau_{\text{eff}} \) is \( \approx 0.16 \) ps, which corresponds to \( f_{\text{max}} \approx 500 \) GHz. At high, negative, gate bias, injection of holes from the drain is facilitated \([11]\), leading to an increase in the quantum-capacitance contribution to \( C_{\text{gd}} \). Thus, assumption equation (15) overestimates \( C_{\text{gd}} \), leading to equation (16) overestimating the true \( \tau_{\text{eff}} \) at the most negative bias considered. The effect of assumption equation (17) is more severe at high bias because \( g_{m} \) falls off considerably. Again, this is due to holes being injected into the nanotube from the drain: the resulting hole flow bucks that issuing from the source, reducing \( g_{m} \). Moreover, \( g_{ds} \) rises in that bias range, ultimately yielding a ratio \( 2g_{ds}/g_{m} \approx 1 \) near \( V_{GS} = -0.8 \) V and invalidating assumption equation (17).

We turn now to device 2, which has a nanotube diameter \( d_{t} = 0.8 \) nm (taken to correspond to a tube of chirality (10, 0)), a positive hole-barrier of 0.3 eV at the Pd end-contacts \([9]\), an increased insulator thickness \( t_{\text{ins}} \) of 8 nm and shorter contacts \( L_{c} \) of 30 nm. The higher barriers and thicker insulator will reduce \( g_{m} \) below that of device 1. These features should lead to a lower \( f_{\text{max}} \) than predicted for device 1. However, this should be mitigated somewhat by lower capacitances \( C_{gs} \) and \( C_{gd} \), due to the larger \( t_{\text{ins}} \) and smaller \( L_{c} \). The results shown in figure 5 show that \( f_{\text{max}} \) is, indeed, significantly lower than for device 1. Interestingly, \( \tau_{\text{eff}} \) is a better approximation to the true \( \tau_{\text{eff}} \) in this case, which is perhaps unexpected, given that the shorter \( L_{c} \) and thicker \( t_{\text{ins}} \) should reduce the inter-electrode capacitances that would otherwise help to equalize \( C_{gs} \) and \( C_{gd} \). The reason lies in the positive barrier heights and larger bandgap, which restrain charge injection into the nanotube (see...
The error in the estimation of the prediction of making assumption (17), and shows that the error is greatest at the source generally reduces the drain current, so both changes reduce the inter-electrode contributions. The higher dependence of Equations (16) and (18) highlight this by elucidating the direct helpful because of its domination of the output admittance.

One of the reasons for the low $f_{\text{max}}$ shown for device 2 in figure 5 is that the effective gate bias is lower than for device 1 because of the higher threshold voltage due to the thicker gate insulator. While this could be ameliorated by application of a higher negative bias to the gate, or by using a higher work function for the gate metal, figure 5 is useful because it illustrates that our equations are reasonable over an effectively different bias range than applies to device 1.

So far, we have used resistances of $R_c \approx 0.9 \, \text{k}\Omega$ and $R_g = 1 \, \text{k}\Omega$. To examine the effect of parametrically changing these values, results are presented in figure 6 for device 1. The error in the estimation of the prediction of $f_{\text{max}}$ was examined, after making each of the assumptions leading to the three expressions for $\tau_{\text{eff}}$. For the first two, the error in $f_{\text{max}}$ is less than 1% over the range of resistances shown in figure 6(a). Figure 6(b) depicts the case after, additionally, making assumption (17), and shows that the error is greatest at large $R_c$. This is because the approximated term, $(g_m+2g_{bs}) \rightarrow g_m$ in simplifying equation (16), is multiplied by the square of $R_c$, whereas $R_g$ appears without exponentiation. Figure 6 indicates that the compact expressions are useful over a wide range of resistance values.

Finally, we demonstrate the utility of the compact expressions in guiding design towards CNFETs that should lead to improved $f_{\text{max}}$. Obviously, reducing $C_{\text{gd}}$ would be helpful because of its domination of the output admittance. Equations (16) and (18) highlight this by elucidating the direct dependence of $\tau_{\text{eff}}$ on $C_{\text{gd}}$. By contrast, $\tau_{\text{eff}}$ has a lesser dependence on transconductance. One way to trade off $g_m$ against $C_{\text{gd}}$ would be to increase $t_{\text{ins}}$. Ways to reduce $C_{\text{gd}}$ directly would be to shorten the drain contact $L_c$, and to increase the gate–drain underlap $L_{\text{ud}}$. Although the functional dependences of $g_m$ and $C_{\text{gd}}$ on $t_{\text{ins}}$ and $L_{\text{ud}}$ are not readily attainable, the beneficial effect to device 1 of making these changes is illustrated in figure 7, where the peak value of $f_{\text{max}}$ is raised by about 15% to 580 GHz.

4. Conclusions

From this study of the extrapolated $f_{\text{max}}$ in Schottky-barrier CNFETs it can be concluded that

(i) compact expressions for $f_{\text{max}}$ can be derived that are useful over wide ranges of physical properties, parasitic resistances and gate biases,

(ii) the compact expressions provide a useful guide to the design of high-frequency devices and

(iii) $f_{\text{max}}$ values in excess of 0.5 THz should be realizable.

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References


